The Implementation of Digital Down Converter System based on Quartus Ⅱ

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Abstract: The main work of DDC is as follows: on the one hand, the wideband signals including all channels are separated to extract the required narrowband signals; on the other hand, for the separated narrowband signals, according to the sampling theorem, the amount of data can be reduced and the processing pressure of baseband part can be relieved. The performance of digital down conversion directly affects the performance of the whole digital demodulator. In this paper, when the input if frequency is variable, the AD sampling rate is changed to adapt to the IF frequency. That is, DDC and DDS are combined. This paper describes the implementation of DDC when the IF signal frequency is from 60MHz to 80MHz and the symbol rate is 1.338m/s. Finally, the performance of digital down converter is simulated by Simulink, and the performance of digital down converter is measured by test circuit under Quartus II.

1. Introduction

Based on the analysis and research of the basic structure and implementation method of digital down conversion, this paper proposes a method to realize DDC by changing the AD sampling rate to adapt to the IF frequency when the input if frequency is variable, and simulates the algorithm proposed in this paper by Simulink, and tests the performance of digital down conversion with the test circuit under Quartus II. This method is suitable for the case of small signal bandwidth. This scheme is simple to implement and saves resources.

2. Working Principle and Key Technology of DDC

The composition of digital down converter is similar to that of analog down converter, including three parts: digital mixer, digital controlled oscillator NCO and low pass filter (LPF), as shown in Figure 1.

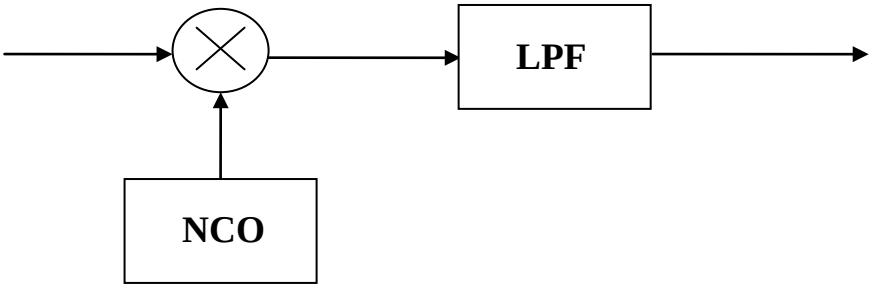


Figure 1. Composition of digital down converter

In terms of spectrum, digital down conversion transforms the input signal from if to baseband. Such processing is completed in two steps: after the quantized if digital signal enters the digital down converter, it first mixes with the local digital signal generated by the digital controlled oscillator (NCO), and then passes through the low-pass filtering, the signal becomes the baseband

signal.

2.1. Digital Controlled Oscillator NCO

Digital controlled oscillator is relatively complex in DDC, and it is also one of the most important factors that determine the performance of DDC. The objective of NCO is to produce a sine wave sample with variable frequency, as follows:

$$S(n)=\cos\left(2\pi \bullet \frac{flo}{fs} \bullet n\right) \quad (n=0,1,2,\ldots) \tag{1}$$

flo is the local oscillation frequency; fs is the sampling frequency of DDC input signal. When DDC is working, NCO will add a phase increment for each sample of signal to be downconverted to DDC, and then take the $2\pi\frac{flo}{fs}$ phase accumulation angle , Then the address is based on the phase accumulation angle $\sum_{i=0}^{n} 2\pi \times \frac{flo}{fs}$ as the address, check the data on the address and output it to the digital mixer, multiply with the signal sample, and the product sample will be output after passing through the low-pass filter, thus completing the digital downconversion.

2.2. Band Pass Sampling Theorem

Set a frequency band limited signal x (t) whose frequency band is limited within (f_L, f_H). To make the sampling signal accurately determine the original signal, the sampling rate fs and the center frequency fo of the band limited signal meet the following requirements:

$$f_s = \frac{4f_0}{2n+1} \quad (n\geq 0) \tag{2}$$

2.3. Half-band Fir Filter

Half band FIR filter is used in low-pass filter. Half band filter is a kind of special linear phase filter. Nearly half of its coefficients are accurate to zero, so its operation amount of filter is reduced by nearly half compared with other linear phase filters of the same length, saving resources.

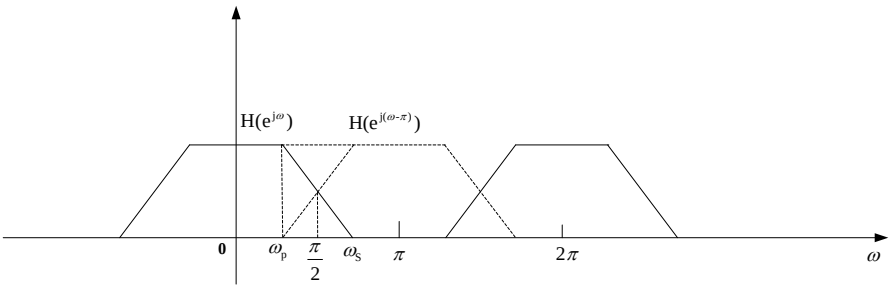


Figure 2. Characteristics of half band filter

3. Realization of Digital Down Conversion

3.1. Simulation of Digital Down Conversion in MATLAB

3.1.1. Specific structure of simulation module

In MATLAB, we use the Simulink simulation tool to simulate the digital down converter, and realize the specific algorithm to verify the correctness of the algorithm. The top structure of DDC is shown in Figure 3.

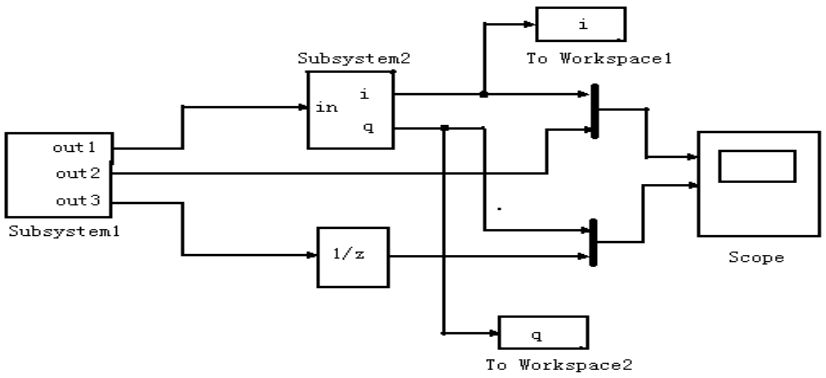


Figure 3. Structure of digital down conversion simulation module

Among them, subsystem 1 is a digital sequence generating module, which generates the real IF signal to be down converted. The digital down conversion module designed in this paper can be applied to all if sampling demodulators. But in the simulation of the digital down conversion system, the binary signal modulated by BPSK is down converted.

Subsystem 2 is the core part of digital down conversion, including mixing and filtering. In the subsystem 2 module, a sinusoidal sample with variable frequency is generated by the digital controlled oscillator. The structure of the module is shown in Figure 4.

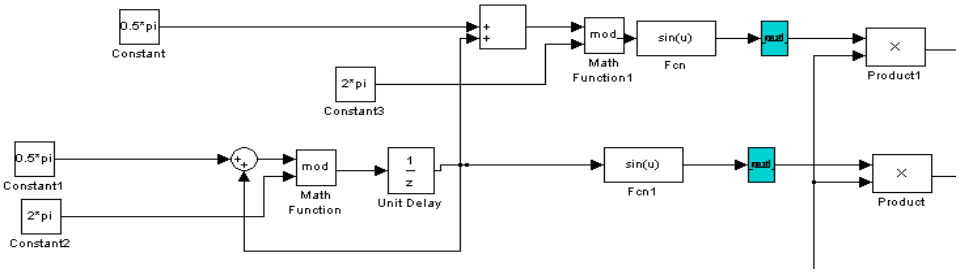


Figure 4. Structure diagram of mixing module

Half band FIR filter is used in the filter. Its characteristic is that half of the coefficient of impulse response is zero. Compared with the anti aliasing filter with ordinary double decimation, the operation amount can be reduced by half and the total operation amount can be greatly reduced. In this paper, a half band filter with 15 order passband width of 2MHz is designed, and the coefficients of the filter are obtained. The structure of half band FIR filter is shown in Figure 5.

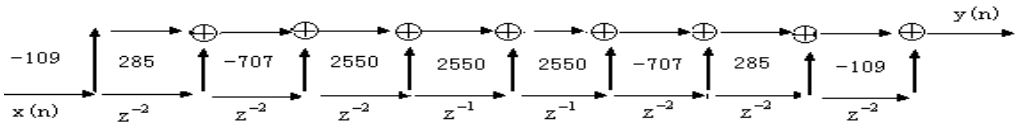
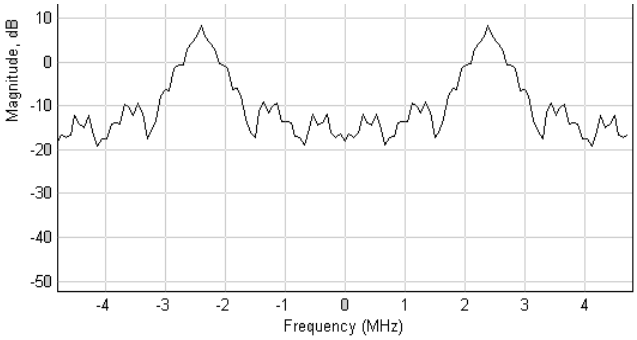


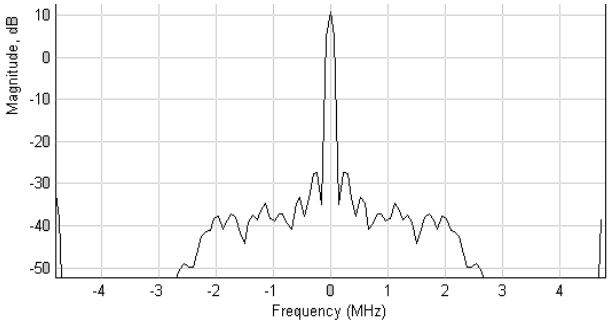
Figure 5. Structure of half band FIR filter

3.1.2. Simulation results of Simulink

The following is the simulation result of Simulink. Figure 6 shows the frequency spectrum of the signal near the zero frequency when the input if is 60MHz (as shown in Figure 6(a)) and the baseband signal after down conversion (as shown in Figure 6(b)).



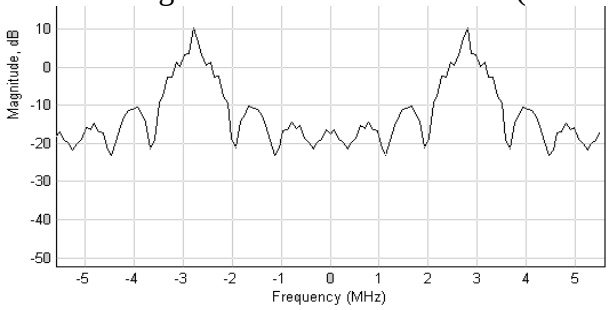
(a). Spectrum of signal near zero frequency when if is 60MHz



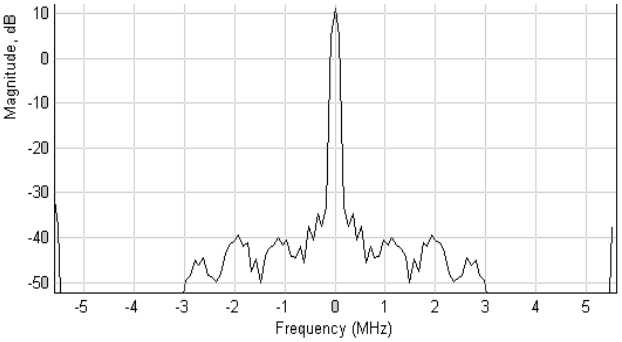
(b). Baseband signal from DDC when if is 60MHz

Figure 6. Simulation results at 60 MHz

Fig. 7 shows the spectrum of the signal near the zero frequency when the input if is 70MHz (as shown in Fig. 7 (a)) and the baseband signal after down conversion (as shown in Fig. 7 (b)).



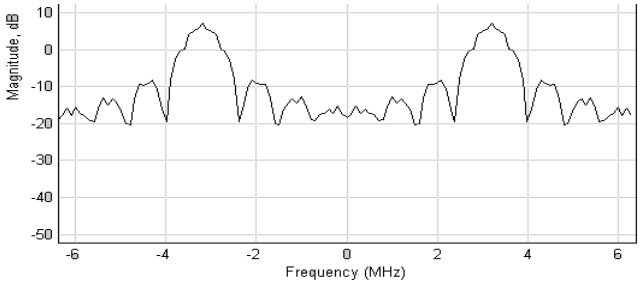
(a). Spectrum of signal near zero frequency when if is 70MHz



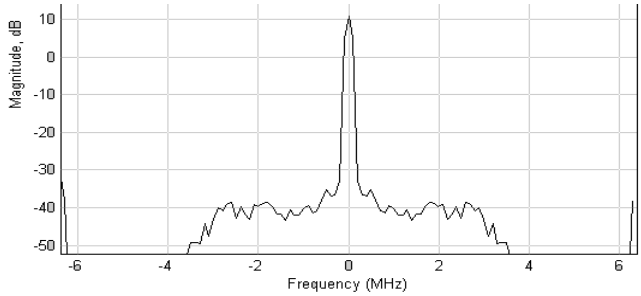
(b). Baseband signal from DDC when if is 70MHz

Figure 7. Simulation results at 70 MHz

Fig. 8 shows the spectrum of the signal near the zero frequency when the input if is 80MHz (as shown in Fig. 8 (a)) and the baseband signal after down conversion (as shown in Fig. 8 (b)).



(a) Spectrum of signal near zero frequency when if is 80MHz



(b) Baseband signal from DDC when if is 80MHz

Figure8. Simulation results at 80 MHz

3.2. Simulation of Digital down Conversion under Quartus Ⅱ

DDC is realized by FPGA. In this paper, Verilog language is used to write the corresponding program, and Quartus II software is used to simulate. In this paper, the signal source generated in MATLAB is used to generate the corresponding MIF file, and then it is imported into the ROM of Quartus II module.

The program is written in Verilog language, and the algorithm used in mixing part is as described in Section 3.1: make the sampling rate 4 times of the small if, and make the sampling value alternate to 0, 1, 0, - 1. In this way, the quadrature I and Q signals can be obtained only by multiplying the values of + 1, 0 and - 1 alternately with the sampling IF signal sequence. There is no need to participate in the oscillation signal of the local numerical control oscillator (NCO), which can greatly reduce the amount of memory required by the chip. After mixing, the baseband signal is obtained by low-pass filtering.

The multiplier design method adopted in this paper is a multiplier free structure, which uses the structure of decomposing coefficient into power of 2, and the multiplication is replaced by shift addition. There are many kinds of algorithms which can be used to design multiplier free structures. Their common feature is to reuse multiplication coefficient operation as much as possible and save logical operation.The simulation structure under Quartus II is as follows:

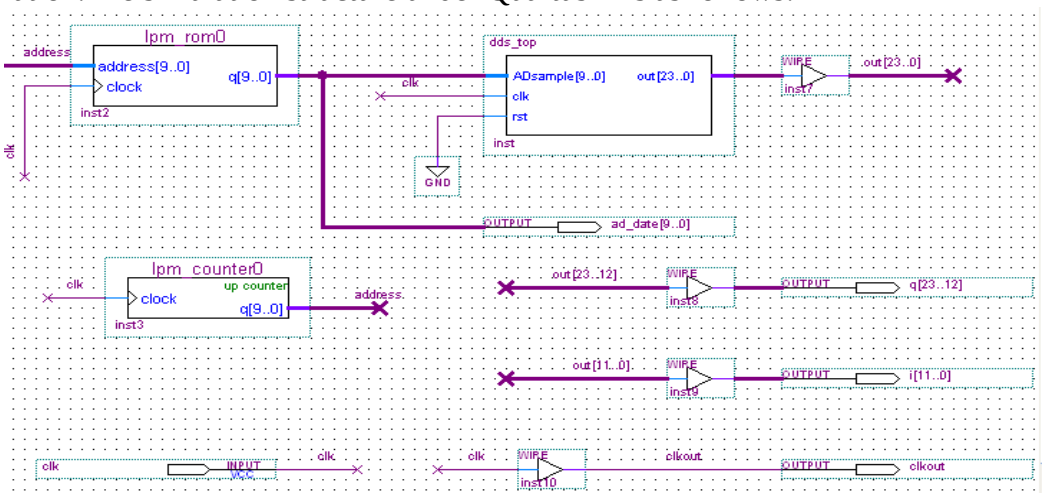


Figure9. Simulation structure under Quartus II

The figure above shows the simulation structure of digital down conversion under Quartus II, in which DDS top is the core module, including mixing module and filtering module. Input if is 70MHz, symbol rate is 1.338m/s, and sampling rate is 11.2mhz. The time series waveform of Quartus II simulation is shown in Figure 10:

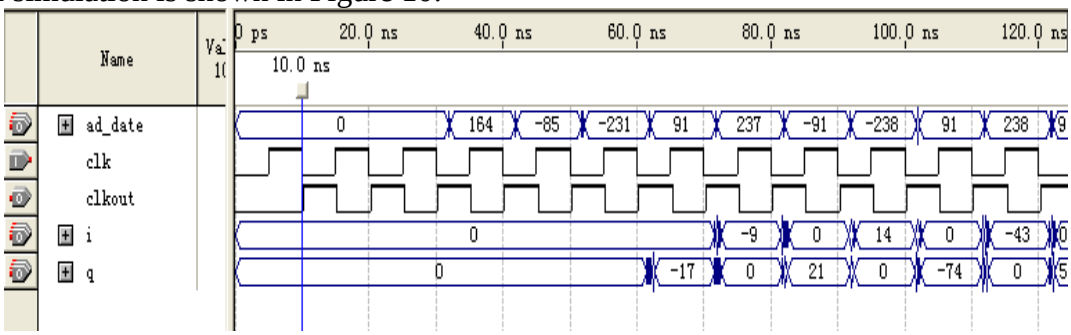


Figure10. Quartus II simulation time series waveform

Where ad_date is the input if digital sequence, I and Q are two output results.We compare the simulation results of time series waveform under Quartus II with the simulation results of MATLAB, and find that they are consistent with each other. Thus, the correctness of the DDC method proposed in this paper is verified by changing the AD sampling rate to match the IF frequency when the input if frequency is variable. This scheme is simple to realize, saving resources, and suitable for the situation of small signal bandwidth.

4. Conclusion

This paper studies the structure, basic working principle and implementation method of digital down converter. This paper proposes a solution to change the sampling rate of IF signal without changing the DDC structure. At the same time, the implementation method of DDC when the IF signal frequency is from 60MHz to 80MHz and the symbol rate is 1.338m/s is described in detail. Finally, the performance of digital down converter is simulated by Simulink, and the performance of digital down converter is measured by test circuit under Quartus II. The test results show that this method has good performance and is easy to implement.

References

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