Design Of FIR Filter Based On FPGA And DSP Builder

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Abstract: Due to advantages in performance, cost, power consumption, etc., signal processing modules based on FPGA and DSP Builder have been widely used in various signal processing fields. At present, FPGAs and DSP Builders generally implement fixed-point number calculations for FIR filters. Due to the limited fixed-point number length, they cannot meet the accuracy requirements. Therefore, FPGAs are used to implement high-speed, high-precision floating-point high-order FIR filters. Very important significance. In this paper, the digital signal processing model is established graphically in MATLAB/SIMULINK environment to design and simulate the DSP BUILDER, and the designed graphic file .mdl is directly converted into a C language program to run in CCS. By adding AD and D/A interface programs, the software can be downloaded to the DSP BUILDER target board after debugging and compilation. This article introduces the advantages of FPGA in digital filter design and application. The inherent flexibility of FPGAs also allows designers to keep up with the changes in the new standards, and can provide feasible methods to meet the changing standards. This article discusses the basic principles of multi-rate signal processing, proposes an improvement of the multi-phase structure, and does some theoretical research on the application of FPGAs in multi-rate signal processing. Research shows that this paper builds a 70-tap linear phase FIR filter as an example, and only requires four 256 input and one 8 input LUT. You can use a simple adder tree to connect their outputs. It can be seen that the fully parallel structure has the best performance, but it also consumes the most resources.

1. Introduction

Since the development and maturity of computers and the accompanying digital signal processing technology, signal spectrum analysis is gradually being replaced by DSP BUILDER [1-2]. With the advent of the information age and the digital world, digital signal processing has become an extremely important discipline and technical field. It is used in communications, voice, imaging, automatic control, radar, military, aerospace, medical and household appliances It has been widely used. In digital signal processing applications, digital filters are very important and are widely used [3-4].

The widespread use of filters in my country was in the late 1950s. At that time, it was mainly used for speech filtering and newspaper filtering [5-6]. After half a century of development, the development, production and application of China's filters have been included in the international development pace. However, due to the lack of special development institutions, the integrated process and material industry cannot keep up, which has led to the development and application of many new filters in China [7-8]. There is a distance for international development. The types of existing filters and the frequencies covered in our country have basically satisfied all kinds of existing telecommunications equipment. Overall, the development of active filters in my country is slower than that of passive filters, and has not yet been mass-produced and applied. The application of various types of filters in China can be seen from the following production and application ratios: LC filters account for 50%; crystal filters account for 20%; mechanical filters account for 15%; ceramics and surface acoustic filters each account for 1%; The remaining types of filters account for 13%. From these application ratios, if my country's electronic products want to achieve large-scale

integration, filter integration is still an important issue [9-10].

This paper uses the MATLAB/SIMULINK function to realize the principles and algorithms of the digital filtering system. It is compiled into a specific specification of C language through MATLAB software. This C language can be compiled into an assembly language of a specific DSP BUILDER chip. The integrated development environment is integrated in the DSP BUILDER chip. —After debugging in CCS, the executable program is burned into the hardware circuit to run to realize the digital filtering function. This article introduces the traditional design method and FPGA design method of linear phase FIR digital filter. This article focuses on the application of distributed algorithms in FIR filters. In order to verify the advantages of distributed algorithms in FPGA digital signal processing, this paper is based on the Quartus II9.1 platform, focusing on the design and implementation of FIR filters based on parallel distributed structure, and verified.

2. Fir Filter Design Based On Fpga And Dsp Builder

2.1. Theoretical Basis Of System Design

Digital filters can be divided into two categories. One is called classic filters. The useful components in the input signal and the components that you want to filter occupy different frequency bands. Filtering can be achieved through appropriate frequency selection filters. FIR and IIR filters are very different in terms of performance and design method. FIR filters can be designed directly according to the given frequency characteristics, while IIR filters need to be designed using general analog filter design methods. But regardless of FIR and IIR, the design steps are as follows:

(1) Determine the index: There must be some indexes before designing a filter, these indexes need to be determined according to the application.

(2) Model approximation: Once the index is determined, a filter model can be proposed to approximate a given index system using some basic principles and relationships. This is the main problem to be studied in filter design.

(3) Implementation: The filter obtained in the above two steps is usually described by the system function of the differential equation or the impulse response. According to this description, it is realized by hardware and computer software.

For many applications, digital filters generally have the following difference equations:

$$y(n) = \sum a_k\, x(n-k) + b_k y(n-k) \tag{1}$$

In the formula, x(n) is the input sequence, y(n) is the output sequence, a_k and b_k are the filter coefficients, if b_k=0, then:

$$y(n) = \sum a_k\, x(n-k) \tag{2}$$

Equation (2) is the difference equation of the FIR filter, without loss of generality, we use below

$$y(n) = \sum a_k x(n-k) \tag{3}$$

To express the difference equation of the FIR filter, perform Z transformation on equation (4), and after finishing, the transfer function of the FIR filter can be obtained:

$$H(z) = \sum h(k) z^{-k} \tag{4}$$

In digital filters, FIR filters have the following advantages:

I) The amplitude characteristics can be arbitrarily designed while ensuring accurate and strict linear phase;

2) Since the unit pulse h(n) of the FIR filter is a finite-length sequence, the FIR filter has no problem of instability;

3) Since FIR filters are generally non-recursive structures, under finite precision calculations, there will be no unstable phenomena such as limit oscillations in recursive structures, and the error is small.

4) The FIR filter can be implemented using the FFT algorithm, thereby improving the operation efficiency. Let the transfer function $H(e^{jw})$ of the digital filter be expressed by the following formula:

$$H\left(e^{jw}\right) = \left|H\left(e^{jw}\right)\right| e^{\epsilon w} \tag{5}$$

$\left|H\left(e^{jw}\right)\right|$ is the amplitude-frequency characteristic, and ϵw is the phase-frequency characteristic.

The amplitude-frequency characteristic represents the attenuation of the frequency component after the signal passes through the filter, and the phase-frequency characteristic reflects the time delay of each frequency component after passing through the filter. In general, the specifications of frequency selection filters are given in terms of amplitude-frequency characteristics, and phase-frequency characteristics are not required. If strict requirements are required for output waveforms, such as speech synthesis and waveform transmission, linear phase digital filters are required.

2.2. Implementation Structure Of Fir Filter On Fpga

A common method of real-time filter is the use of software programmable DSP BUILDER chip. It can also be implemented with ASIC, but it is a high-performance but less flexible alternative. The latest design method is to use the pipeline processing method based on the online programmable hardware system. The simulation of several classic FIR filters in Quartus II will be discussed in detail below.

(1) Implement FIR filter structure based on MAC

There are many ways to implement FIR filters in FPGAs. The most obvious but not the best way is to imitate the technology used in ASIC or instruction set DSP BUILDER (ISDSP BUILDER). This method uses a preset multiply-accumulator (MAC) unit.

The theoretical basis of this method is that the inner product calculation can be divided on one or several MAC units, which is a method commonly used in current signal processors (ASIC and ISDSP BUILDER). This method is also applicable to the design of digital filters implemented by FPGA, but in the FPGA environment, the designer has complete control over the silicon and can determine how much resources are allocated to the inner product engine. When evaluating a particular filter implementation technology, designers need to consider some necessary factors, such as performance (sampling rate), power consumption, size, and cost. In order to give a reference framework for FPGAFIR filter implementation, we will compare the MAC-based FPGAFIR filter implementation method with the ASIC and ISDSP BUILDER methods. First consider the ASIC scheme provided by the DSP BUILDER-24 DSP BUILDER-24 signal processor. This device can achieve a variety of functions, including filtering. DSP BUILDER-24 uses a 100MHz clock frequency and 24-bit data and coefficients to complete a real filter tap calculation within 5ns and a complex tap calculation within 10ns.

(2) FIR filter based on DA algorithm

In many systems, the coefficient set of the filter is symmetrical, and symmetry can be used to reduce the need for logic chips by half of the filter design. For 24-bit input sampling, the sampling rate is 4.1666MHz. At this time, the filter rate is slightly reduced. For 24-bit input sampling and 100MHz clock, the sampling rate will be 4MHz. For a 200-tap filter, the calculation rate of 800MMAC per second will still be obtained.

3. Experimental Design of FIR filter Based on FPGA and DSP Builder

3.1 Initial Setup

The C language program generated by the MATLAB graphics file automatically calls the CCS2 software to compile and run the project file. The program directly generated by MATLAB can realize the digital filtering function, but because of the many default settings used in the program, there are still some problems in the process of running. In the program generated by the above method, only the timer interrupt is processed in the interrupt handler. When other interrupts are caused by interference signals, it will cause DSP BUILDER to stop. Therefore, define an invalid interrupt (_nothing) in the interrupt vector and add an interrupt service routine 1x1 in the interrupt response program. Other functions also need to be debugged to run properly. For example, A/D_CS is controlled by IOPA5 and D/A_CS is controlled by IOPA4. Therefore, it is necessary to configure the write parameters of registers MCRB and PADATDIR and realize the conversion timing of AD and D/A.

3.2 Data Reading Module

This module converts externally sampled data into an address and reads it into subsequent modules for processing to prepare for subsequent circuits. The specific operation is to differentiate the first bit of the original 8-bit address line from the last 3 bits or to obtain a new address bus, and at the same time, it can also be used as an enable signal for the subsequent LUT to select the subsequent LUT; in this structure The coding methods of the two LUTs are the same to ensure the simplicity of operation. indata is the address line data input; outdata is the address line output, which is used as the address input of the lookup table.

3. 4. Analysis of FIR Filter Experimental Design Based on FPGA and DSP Builder

4.1 Fir Filter Based On Parallel Distributed Algorithm

Another way to implement DA LUT in distributed memory is to use the memory module in the new generation FPGA. Taking the construction of a 70-tap linear phase FIR filter as an example, only 35 dedicated filter parameters are needed, and a simple LUT method needs to store a large number of partial product terms. If 35 address lines are divided into 4 groups of 8 addresses and 1 group of 3 addresses, it is easier to manage. Only 4 256 input and 1 8 input LUT are needed. These 5 lookup tables can be stored in the on-chip storage module, and then a simple adder tree is used to connect their outputs. Through VHDL simulation in the Quartus II environment, the data performance comparison of various serial and parallel algorithms is shown in Table 1.

Table 1. Performance comparison of various algorithms

Filter Type	Pipeline Level	DSP BUILDER Blocks	M512	M4K	LEs	fmax	MSPs
Serial	2	1	5	8	235	374	44.23
Parallel	2	0	0	34	1593	423	412
Multi-cycle variable	1	3	13	423	2412	188	187

Table 1 shows the detailed resource occupancy. It can be seen that the fully parallel structure has the best performance, but it also occupies the most resources. In specific applications, the algorithm must be selected according to the hardware resources and the real-time requirements of the system.

4.2 Matlab To Quickly Establish Ti Dsp Builder Model Experiment Analysis

In this paper, the anti-interference ability has been significantly improved after adopting FIR filtering. The method of quickly establishing the TI DSP BUILDER model and directly generating the C language program using MATLAB simplifies the development of the DSP BUILDER software. It is also included in the Embedded target for TI C2000 toolbox In addition to other tools, such as PWM control, CAN bus control and general I/O control, etc., these tools can be combined with other T-boxes in SIMULINK to complete complex function DSP BUILDER programming, and only a small amount of additions and modifications are required , You can achieve the correct function of the C language program design, saving program writing and input time. The above design has been confirmed in the hardware circuit, and the schematic diagram has been made into PCB. It has been experimentally proved that this design method accelerates the development cycle than writing the program directly in CCS, and the filtering effect is obvious.

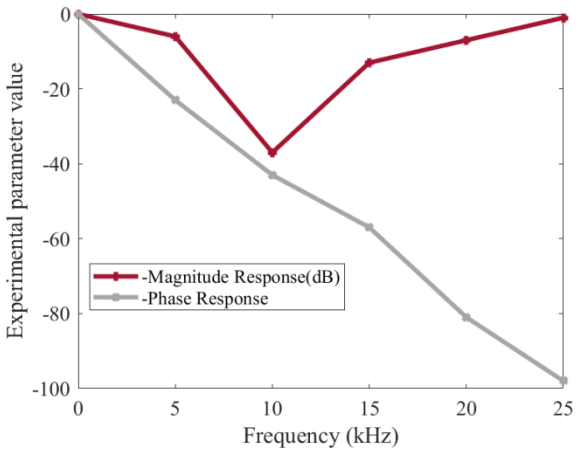

Figure 1. Filter phase-frequency response curve

As can be seen from the amplitude-frequency response curve, the passband, stopband, passband ripple, and stopband attenuation of the filter all meet the design requirements. It can be seen from the phase frequency response curve that the phase response of the FIR filter can be strictly linear, so it has no delay distortion and only a fixed time delay. It is suitable for image signal processing, data transmission, and other systems that carry information with waveforms. FIR filters overcome the shortcomings of analog filters and IIR digital filters that only consider the amplitude-frequency characteristics and not the phase characteristics. To obtain a linear phase, a phase correction network must be added to make the filter complicated. While the FIR filter ensures that the amplitude-frequency characteristics meet the technical requirements, it is easier to achieve strict linear phase.

Conclusions

The first is to broaden the application field. Many devices that used analog signal processing in the past are now trying to use digital signal processing instead. Including communications, voice processing, radar and sonar signal processing, radio and television technology, biological and medical signal processing, seismic and geographic information, transportation and industrial control. Tens of thousands of special integrated circuit chips for signal processing have emerged, making the speed of digital signal processing rapidly increasing, while its cost has been continuously reduced. The principle of distributed algorithm and the construction method of lookup table gradually introduce a multiplier based on pipeline distributed algorithm. Through analysis and comparison, it is concluded that this multiplier based on pipelined distributed algorithm is superior to traditional multipliers in performance and other aspects. Then according to this algorithm idea, we designed a 17th order FIR filter.

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